HIGH EFFICIENCY GaAs-on-Si SOLAR CELLS WITH HIGH V_{OC} USING GRADED GeSi BUFFERS

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ABSTRACT

Single junction AlGaAs/GaAs and InGaP/GaAs solar cells and test structures have been grown by molecular beam epitaxy (MBE) and metalorganic chemical vapor deposition (MOCVD), respectively, on Si wafers coated with compositionally-graded GeSi buffers. The combination of controlled strain relaxation within the GeSi buffer and monolayer-scale control of the III-V layer nucleation is shown to reproducibly generate minority carrier lifetimes exceeding 10 nanoseconds within GaAs overlayers. The III-V layers are free of long-range anti-phase domain disorder, with threading dislocation densities in the high-10^5 cm^{-2} range, consistent with the low residual dislocation density in the Ge cap of the graded buffer structure. Single junction GaAs cells grown by both MBE and MOCVD on the Ge/GeSi/Si substrates demonstrated high Voc values for GaAs cells grown on Si. Record Voc values for MOCVD-grown single junction InGaP/GaAs cells exceeded 980 mV (AM0) with fill factors of 0.79. Additionally, external quantum efficiency data indicates no degradation in carrier collection from GaAs homoepitaxial cells for current single-junction cell designs grown by MBE. Based on these results, cell efficiencies in excess of 18.5% under AM0 conditions should be attainable with cell designs demonstrating state of the art J_{sc} values. Such cell performance demonstrates the potential and viability of graded GeSi buffers for the development of III-V cells on Si wafers.

INTRODUCTION

III-V solar cells for space applications are currently grown on Ge wafers due to the lower cost and somewhat increased mechanical strength of Ge compared to GaAs substrates, coupled with the reasonable lattice match between Ge and GaAs. However, from solely a substrate perspective, Ge is not an optimum substrate material, especially when compared with Si, which is far cheaper, stronger, lighter and available in much larger areas than Ge. In essence, the choice of Ge as the preferred substrate is a compromise, one which results from the need for matching the lattice constant of the III-V overlayers so that high quality, crystalline III-V layers can be grown by epitaxial techniques, resulting in the fabrication of high efficiency cells. Si, unfortunately, while possessing superior substrate properties (low mass density, high thermal conductivity, inexpensive, mechanically strong), is not lattice matched to GaAs and the related III-V alloys that are optimum for solar energy conversion. Indeed, the 4% lattice constant mismatch between GaAs and Si causes very high threading dislocation densities for GaAs directly grown on Si, rendering the GaAs useless as a photovoltaic material. Nevertheless, many groups have recognized the potential benefits of achieving efficient III-V cells on Si and many methods to control and reduce the dislocation density have been investigated to deal with the mismatch problem. Most notably, these include thermally-cycled growth of the III-V intermediate layers and the insertion of various types of III-V buffer layers prior to cell deposition. Each has been successful in reducing the density of threading dislocations from ~ 10^9-10^{10} cm^{-2} for direct epitaxy of GaAs on Si, to ~ mid 10^6 cm^{-2} – mid 10^7 cm^{-2}.[1-6] However, this dislocation density has still limited the minority carrier lifetimes obtained to ~ 1-3 ns, even after hydrogen passivation [5,6], which is not high enough to support efficient III-V solar cells.

As can be seen from the past two decades of activity in the field, almost all efforts to achieve GaAs based solar cells on Si have involved a form of strain management and dislocation engineering within the III-V layers themselves. It is interesting to note that the "optimal" conditions for each approach have tended to result in similar dislocation densities and carrier lifetimes for the GaAs heteroepitaxial layers. This observation implies that limitations may exist within the III-V system in mitigating this large lattice mismatch, which is only exacerbated by the large area requirements for solar cells. This has motivated an alternative approach in which the surface lattice constant of the Si substrate itself is engineered prior to III-V growth, rather than dealing with the mismatch only within the III-V regions. In this way, the lattice mismatch can be addressed in a material system and under growth conditions that are independent from

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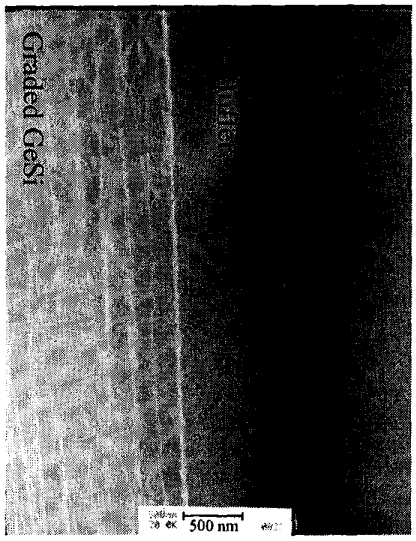

Fig. 1: Representative cross-sectional TEM micrograph of an AlGaAs/GaAs solar cell structure grown on a Ge/GeSi/Si substrate. The upper part of the GeSi graded buffer is shown, along with the lower portion of the GaAs device structure.

Table I: Compilation of lifetime data for 29 DH samples with similar growth conditions (n=1x10^{17} cm^{-3}). GaAs buffer thickness indicates the proximity of the GaAs DH to the GaAs/Ge interface. In all cases, APD formation was suppressed. [13]

Sample	Substrate	GaAs buffer thickness (μm)	S (cm/s) (T=300K)	τ_P (ns) (T= 300K)
A-C	Ge#	0.1	9 x10^3	19.0
D-F	Ge	0.1	2.9 x10^3	19.4
G-I	Ge	0.5	2.8 x10^3	17.2
J-L	Ge/GeSi/Si	1.0	3.9 x10^3	7.7
M-O	Ge/GeSi/Si	0.5	1.3 x10^3	6.6
P-R	Ge/GeSi/Si	0.1	2.2 x10^3	8.3
S-U	Ge/GeSi/Si	0.1	1.9 x10^3	6.4
V-X	Ge/GeSi/Si	0.1	1.9 x10^3	6.8
Y	Ge/GeSi/Si	0.1	2 x10^3 *	9.4
Z	Ge/GeSi/Si	0.1	2 x10^3 *	10.5
AA	Ge/GeSi/Si	0.1	2 x10^3 *	8.6
BB	Ge/GeSi/Si	0.1	2 x10^3 *	8.5
CC	Ge/GeSi/Si	0.1	2 x10^3 *	7.9

#Indicates substrates without UV-Ozone treatment.
*Indicates samples where multiple data points were not available. For these cases, τ_P was calculated assuming S = 2x10^3 cm/s.

the III-V device layers. Hence, a wider range of growth conditions (temperature, growth rate, etc.) may be accessible to achieve optimal lattice relaxation than can be provided by the III-V layers. The Ge_xSi_{1-x} alloy system is well-suited for this application since by increasing the Ge content (x) during growth of a Ge_xSi_{1-x} epitaxial layer on Si, the lattice constant can be increased from that of Si to Ge, providing a close lattice match for subsequent GaAs-based device growth. Indeed recent work has shown that threading dislocation densities (TDD) of less than 1x10^6 cm^{-2} in relaxed Ge layers grown on compositionally-graded Ge_xSi_{1-x} buffers on Si have already been achieved.[7] Moreover, when combined with monolayer-scale control of GaAs nucleation to eliminate the anti-phase domain disorder associated with the GaAs/Ge interface, minority carrier lifetimes in excess of 10 ns for GaAs on Si have been demonstrated. [8,9]

In this paper, we discuss the growth, properties and early cell results of the high lifetime GaAs grown on $Ge/Ge_xSi_{1-x}/Si$ substrates. We show that the growth conditions used to generate high carrier lifetimes also results in negligible diffusion of As, Ga and Ge across the GaAs/Ge interface above the GeSi/Si substrate. GaAs diodes fabricated on Ge/GeSi/Si, Ge and GaAs substrates display nearly identical forward and reverse dark I-V characteristics, indicating that dislocations are not impacting current transport to a first order. Single junction AlGaAs/GaAs and InGaP/GaAs cells were grown by molecular beam epitaxy (MBE) and metal organic chemical vapor deposition (MOCVD), respectively, on these substrates and the highest AM0 Voc values reported to date were achieved for GaAs on Si cells, with very high reproducibility. Record Voc values in excess of 980 mV with fill factors of 0.79 are found. Based on these results, AM0 efficiencies are projected to exceed the current record for GaAs/Si of 18.3% for state of the art single-junction cell designs, indicating the promise and viability of III-V cell development on Si via GeSi buffers.

EXPERIMENTAL

AlGaAs/GaAs and InGaP/GaAs epitaxial layers, double heterostructure (DH) lifetime structures, and single junction solar cells were grown by solid source MBE and by low pressure MOCVD, respectively, on 6° offcut (001) Ge/GeSi/Si substrates. The GeSi buffers were grown by compositional step grading from x = 0 (Si) to x = 1 (Ge) at an average rate of 10% Ge/μm using ultra high vacuum chemical vapor deposition (UHVCVD) as described previously.[7] Plan-view and cross sectional transmission electron microscopy (TEM), electron beam induced current (EBIC), and etch pit density (EPD) measurements confirmed an average TDD = 0.8 – 1.5x10^6 cm^{-2} present in the relaxed Ge cap layer for a large number of growth runs, a direct result of the reduction in threading dislocation pile-ups during the growth of the graded GeSi buffer. Prior to III-V growth, the Ge/GeSi/Si substrate surfaces were cleaned and oxide etched prior to a UV-ozone exposure. For growth on Ge/GeSi/Si and Ge substrates, GaAs growth was initiated with a short migration enhanced epitaxy (MEE) step via MBE and was followed by conventional epitaxial growth. All AlGaAs/GaAs structures were grown using MBE as described previously,[9-11] whereas all InGaP/GaAs structures were grown using a low pressure MOCVD

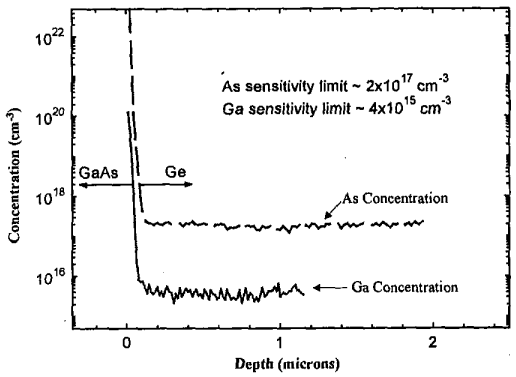

Fig. 2: SIMS data indicating minimal diffusion of Ga and As across the GaAs/Ge interface for GaAs growth on a Ge/GeSi/Si. Ga and As concentrations across the interface are below the SIMS detection limits of $3x10^{15}$ and $2x10^{17}$ cm^{-3}, respectively. Diffusion of Ge into the GaAs layer also was below SIMS detection limit of $3x10^{16}$ cm^{-3} (not shown).

reactor at a substrate temperature of 650°C. Bulk minority carrier lifetimes (300 K) were extracted from the DH AlGaAs/GaAs structures that were nominally doped at n = $1x10^{17}$ cm^{-3} using time-resolved photoluminescence (TRPL) as described in earlier work.[8,12] Cell structures were processed and evaluated by dark I-V, light I-V and spectral response measurements under AM0 conditions. Cr-Au was used for all p-type GaAs contacts. N-type contacts for Ge and GaAs were Au/Sb while Al was used for Ge/GeSi/Si. A triple layer $MgF_2/ZnS/MgF_2$ anti-reflection coating was used for all cells. Identical cells and diodes were grown on Ge/GeSi/Si, Ge and GaAs substrates to compare devices as a function of substrate choice.

RESULTS AND DISCUSSION

Structural and minority carrier properties in GaAs on Ge/GeSi/Si Substrates

We have previously found that threading dislocations are not observable within MBE-grown AlGaAs/GaAs cell structures grown on the Ge/GeSi/Si substrates at the scale of cross-sectional TEM, and that lower magnification methods are needed to approximate threading dislocation densities.[8] Hence, using a combination of lower magnification tools, including electron beam induced current (EBIC), plan-view TEM and etch-pit density (EPD) measurements, the III-V layers were found to contain a TDD of $0.8\text{-}1.5x10^6$ cm^{-2}, identical to the underlying Ge cap of the GeSi/Si substrate. This suggests that the GaAs/Ge interface is behaving as an "ideal" low-mismatched interface and generates, at most, only a very low density of new dislocations during III-V growth. That is, the threading dislocation density within the III-V device layers is essentially a result of the residual TDD within the Ge cap on the graded GeSi buffer. Hence, the Ge/GeSi/Si structure behaves as a "virtual Ge" substrate, i.e. a Si substrate but one with a surface lattice constant of Ge. Moreover, as seen from the representative TEM micrograph in figure 1, anti-phase domain (APD) disorder is either completely eliminated or, when an initial MEE step is not used, self-annihilates within ~10 nm of growth. In either case, no APD disorder is detected beyond the first 10 nm of GaAs growth on the Ge surface. These results are identical to our earlier observations for optimal MBE growth of GaAs on Ge wafers,[9-11] indicating the similarity of GaAs growth behavior on Ge-coated Ge/GeSi/Si substrates and Ge wafers.

The excellent structural properties of GaAs grown on Ge/GeSi/Si substrates are manifested in the observation of very high minority carrier lifetimes for AlGaAs/GaAs/AlGaAs DH structures. Table I shows a compilation of bulk n-GaAs minority carrier lifetimes obtained from TRPL investigations of AlGaAs/GaAs DH structures from multiple independent growth runs. The bulk lifetimes were calculated from TRPL measurements by obtaining the TRPL decay times as a function of GaAs layer thickness, so that contributions from AlGaAs/GaAs interface recombination could be taken into account.[12] All lifetime measurements were done at 300 K. Note that the values are obtained for DH structures nominally doped to $1x10^{17}$ cm^{-3} to match typical base doping levels within actual cells. As seen from Table I, lifetimes in excess of 7-8 ns are routinely obtained, with a maximum value of 10.5 ns. These are the highest carrier lifetimes observed for GaAs grown on a Si substrate to date. The data compiled in Table I also demonstrate that these results are extremely reproducible, and are relatively insensitive to minor changes in growth initiation conditions, as shown.

Also, from Table I, it can be seen that the measured lifetimes are insensitive to the thickness of a GaAs buffer layer inserted between the substrate and the DH region. No lifetime degradation is observed as the thickness of this layer is reduced from 1 μm to 0.1 μm. We can thus conclude that the GaAs material is of high electronic quality after only 0.1 μm of growth on the Ge/GeSi/Si substrates, verifying the suppression of APD's and control of the low mismatched GaAs/Ge interface. This is significant since it is desirable to minimize the thickness of any inactive III-V layer grown on the Ge/GeSi/Si substrates in order to minimize stresses resulting from thermal expansion mismatch between the III-V layers and the underlying Si wafer which can result in epilayer cracking and wafer bow. [14,15]

However, while the electronic quality of the GaAs material grown on the Ge/GeSi/Si buffer is the most important aspect for photovoltaic performance, the ability of a 0.1 μm GaAs buffer nucleation to minimize cross-diffusion at the GaAs/Ge interface is also important. This has proven to be important issue for GaAs grown on a Ge terminated substrate since the growth temperatures of conventional epitaxy may cause cross diffusion of As, Ga and Ge at the GaAs/Ge interface, generating high background doping over many microns, or even type conversion. In previous work on GaAs growth on Ge

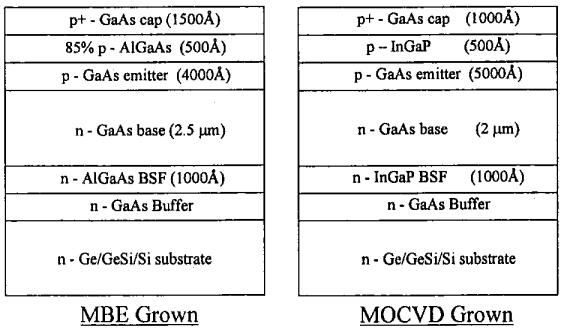

Fig. 3: Device structures for MBE-grown AlGaAs/GaAs and MOCVD-grown InGaP/GaAs p^+n cell structures grown on Ge/GeSi/Si substrates.

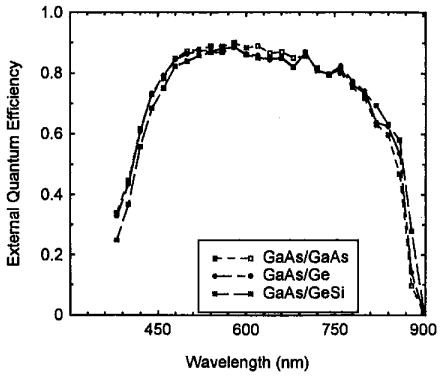

Fig. 4: External quantum efficiency measurements for single junction AlGaAs/GaAs cells grown by MBE on Ge and Ge/GeSi/Si substrates indicating the similar minority carrier collection efficiency for each.

wafers by MBE, we demonstrated the successful minimization of such diffusion to negligible levels using an optimum interface nucleation procedure.[11] Figure 2 shows SIMS concentration profiles for Ga and As across the GaAs/Ge interface for a 2.5 μm thick GaAs layer grown on a Ge/GeSi/Si substrate indicating similar interface control using a similar MBE nucleation methodology. There is negligible diffusion across the interface boundary for all cases (including for Ge out diffusion – not shown), with each element (Ga, As and Ge) below their respective SIMS detection limits of $3x10^{15}$, $2x10^{17}$ and $3x10^{16}$ cm^{-3}. This data indicates that the interface formation conditions are robust enough to ensure that negligible diffusion occurs even after growth of thick III-V layers at conventional MBE growth temperatures (620 °C). Hence, the minimally thick, 0.1 μm, GaAs buffer layer is adequate to simultaneously yield very high GaAs lifetimes and to protect an overlying III-V cell from diffusion and autodoping effects. This also implies that complete control of subsequent cell polarity (p on n versus n on p) and elimination of inadvertent junction formation is possible on the Ge/GeSi/Si substrates.

Single junction solar cells on Ge/GeSi/Si via MBE and MOVCD

P^+n AlGaAs/GaAs and InGaP/GaAs heteroface, single junction cell structures were grown on the Ge/GeSi/Si substrates, using MBE and MOCVD, respectively. The cell structures are depicted in Figure 3. (Note: No attempts to optimize the cell structures have yet been made.) All devices were grown using a 0.1 μm GaAs buffer as discussed above. To assess the influence of the Ge/GeSi/Si substrate on device properties, identical AlGaAs/GaAs structures were grown on GaAs, Ge, and Ge/GeSi/Si substrates by MBE. 1 mm^2 diodes grown on each substrate demonstrated nearly identical I-V characteristics, with turn-on voltages of ~ 1 V for all cases, and identical reverse leakage currents out to at least –2 volts, with a value of less than 15 nA at –2 V in each case. Reverse saturation current densities (J_o) were ~2.0 $x10^{-12}$, ~5.0 $x10^{-11}$, and ~1.0 $x10^{-10}$ A/cm^2 for the GaAs, Ge, and Ge/GeSi/Si substrate respectively, with ideality factors (n) of ~1.5, ~1.5 and ~2.0 respectively. The similar current characteristics indicate that the residual TDD of ~ $8x10^5$ cm^{-2} - $1x10^6$ cm^{-2} in the cell structures on Ge/GeSi/Si are not introducing significant shunt or recombination currents in these diodes that would otherwise significantly lower the diode turn on voltage and increase the reverse leakage current and suggests that shunt currents in a completed, GaAs cell on Ge/GeSi/Si should not be significantly impacted by threading dislocations at our current threading dislocation density.

To verify this, MBE-grown AlGaAs/GaAs and MOCVD-grown InGaP/GaAs single junction cells were fabricated and evaluated. Figure 4 depicts a comparison of the external quantum efficiency (EQE) responses of AlGaAs/GaAs cells fabricated on Ge/GeSi/Si substrates, along with EQE curves for identical AlGaAs/GaAs cells grown on GaAs and Ge wafers. The comparison indicates that the carrier collection efficiency is virtually identical for GaAs cells on either substrate. Hence, the high lifetime observed in the GaAs DH structures discussed earlier is replicated in the cell growth and maintained during the entire cell fabrication process. This is even more significant if one considers that only a 0.1 μm GaAs buffer was used between the cell layers and the substrate, demonstrating the robustness of our interface nucleation process.

However, due in part to the growth rate limitations, MOCVD is the preferred growth technique over MBE for industry production applications. Therefore, in order to investigate the impact of MOCVD growth on GaAs/Ge/GeSi/Si device characteristics, initial InGaP/GaAs single junction cells were also grown on GaAs, Ge, and Ge/GeSi/Si substrates by MOCVD. Figure 5 shows EQE data comparing identical cell structures grown on each substrate. Similar to that seen in figure 4 for MBE growth, in comparison to the Ge substrate, there is no apparent degradation in the carrier collection on the

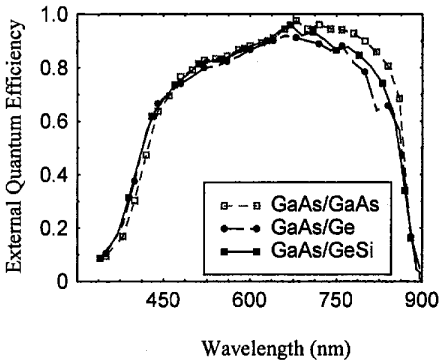

Fig. 5: External quantum efficiency measurements for single junction InGaP/GaAs cells grown by MOCVD on GaAs, Ge and Ge/GeSi/Si substrates indicating the similar minority carrier collection efficiency for each.

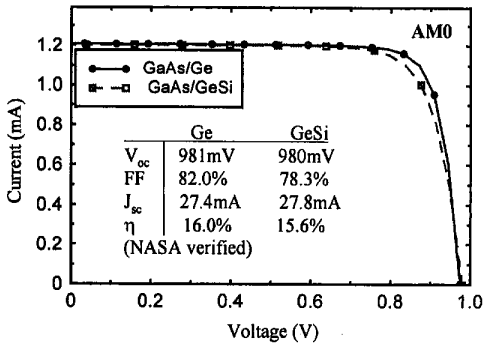

Fig. 6: Light I-V response under AM0 conditions for representative single junction InGaP/GaAs cell (0.2 x 0.2 cm^2) grown on Ge/GeSi/Si substrates (courtesy of NASA Glenn Research Center).

Ge/GeSi/Si substrate due to increased threading dislocation density. However, unlike that seen for MBE growth, a reduction in the collection of long wavelength photons (~700-900 nm) in comparison to the GaAs/GaAs MOCVD growth is apparent. This reduction is attributed to the increased wafer handling due to the sequential use of multiple growth techniques at this preliminary stage of development. Figure 6 shows a typical AM0 light I-V response for both GaAs/Ge and GaAs/GeSi/Si, 2 x 2 mm^2 single junction cells grown by MOCVD. Note that the reduced J_{sc} values (~27.5 mA/cm^2), in addition to the small reduction in the long wavelength carrier collection, are a direct result of the increased metal coverage (due to current small area design) and the single-junction cell structure design itself, which has not been optimized.

However, by far the most notable finding is the very high and very uniform Voc values obtained for these MOCVD grown GaAs/Ge/GeSi/Si cells. Similar to minority carrier lifetime, fill factor, and efficiency, theory presented by M. Yamaguchi et. al. predicts that increased threading dislocation densities will result in a reduction in V_{oc} as diffusion length decreases and recombination current increases.[16,17] Therefore, similar to the record minority carrier lifetimes achieved on the Ge/GeSi/Si substrates due to the improved TDD, theory suggests that these low threading dislocation densities should also result in higher open circuit voltages than those previously attained for GaAs-on-Si.

Indeed, as shown in figure 6, V_{oc} values exceeding 980 mV have been realized for GaAs/Ge/GeSi/Si, the highest reported for an epitaxially grown GaAs cell on a Si wafer under AM0 (NASA-verified) conditions. However, figure 6 also suggests that the Ge/GeSi/Si substrate is not currently limiting the MOCVD grown device performance. Similar to the reduction in the long wavelength collection for the GaAs/Ge and GaAs/Ge/GeSi/Si substrates, the V_{oc} values achieved on these substrates are lower than that achieved for GaAs/GaAs growth of an identical cell structure, ~1060 mV. Since both J_{sc} and V_{oc} values obtained on the Ge/GeSi/Si substrate are identical to those for GaAs/Ge growth, the light I-V and EQE responses indicate that the state of our MOCVD growth development is currently limiting device performance and not the increased GeSi threading dislocation density.

However, the first attempts to transfer our current MBE growth results to MOCVD has still resulted in the realization of record GaAs/Si V_{oc} values. Over 50 cells (2 x 2 mm^2) fabricated across an ~7 cm^2 Ge/GeSi/Si substrate resulted in an average Voc value of ~959 mV. The Voc distribution is depicted in Figure 7. Even though the cell areas were small (2 x 2 mm^2) (so that ample device supply could be generated for research opportunities) the excellent uniformity of cell performance over the large area substrate indicates the outstanding promise for generating larger area cells.

CONCLUSIONS

High quality AlGaAs/GaAs and InGaP/GaAs materials and single junction cells were grown by MBE and MOCVD, respectively, on Ge/GeSi/Si substrates. Minority carrier lifetimes in excess of 10 ns were obtained. APD disorder and atomic diffusion across the heterovalent GaAs/Ge interface were suppressed to negligible levels using only a minimal 0.1 μm GaAs buffer. The high structural and electrical quality of the III-V layers has resulted in carrier collection (EQE) comparable to GaAs/GaAs and GaAs/Ge for the GaAs/GeSi devices via MBE while the current growth methods indicate a reduction in the GaAs/Ge and GaAs/GeSi/Si MOCVD material quality due to the early stages of our MOCVD development. However, MOCVD growth has been shown to result in the highest Voc values reported to date for heteroepitaxial GaAs cells on Si substrates. The excellent performance and uniformity of a large number of cells over large areas of substrate indicates great promise for the generation of very efficient MOCVD grown III-V cells on Si by utilizing graded GeSi buffers.

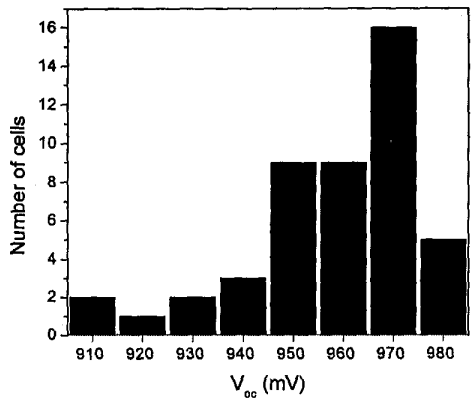

Fig. 7: Histogram of Voc (AM0) distribution obtained for 2 x 2 mm^2 cells distributed across a large area (~7 cm^2) Ge/GeSi/Si substrate. The highest Voc value previously reported for single junction GaAs cells on Si was 0.95 V. [18]

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REFERENCES

[1] M. Yamaguchi, J. Mater. Res. **6**, 376 (1991).

[2] R.K. Ahrenkiel, M.M. Al-Jassim, B. Keyes, D. Dunlavy, K.M. Jones, S.M. Vernon, and T.M. Dixon, J. Electrochem. Soc. **137**, 996 (1990).

[3] R. Venkatasubramanian, M.L. Timmons, J.B. Posthill, B.M. Keyes, and R.K. Ahrenkiel, *J. Cryst. Growth* **107**, 489 (1991).

[4] A. Freundlich, M. Leroux, J.C. Grenet, A. Leycuras, G. Neu, and C. Verie, *Proc. 8th Eur. Comm. Photovoltaic Solar Energy Conf.*, 1522 (1988).

[5] T. Soga, M. Kawai, K. Otsuka, T. Jimbo, and M. Umeno, *Proc. 2nd World Conf. on Photovoltaic Solar Energy Conversion*, 3733 (1998).

[6] G. Wang, G.Y. Zhao, T. Soga, T. Jimbo and M Umeno, Jpn. *J. of Appl. Phys. Part 2*, **37**, L1280 (1998).

[7] M.T. Currie, S.B. Samavedam, T.A. Langdo, C.W. Leitz and E.A. Fitzgerald, *Appl. Phys. Lett.* **72**, 1718 (1998).

[8] R.M. Sieg, J.A. Carlin, J.J. Boeckl, S.A. Ringel, M.T. Currie, S.M. Ting, T.A. Langdo, G. Taraschi, E.A. Fitzgerald and B.M. Keyes, *Appl. Phys. Lett.* **73**, 3111 (1998).

[9] R.M. Sieg, S.A. Ringel, S.M. Ting, E.A. Fitzgerald and R.N. Sacks, J. Electron. Mater. 27, 900 (1998).

[10] R.M. Sieg, S.A. Ringel, S.M. Ting and E.A. Fitzgerald, *Proc. 26th IEEE Photovolt. Spec. Conf.*, 793 (1997).

[11] R.M. Sieg, S.A. Ringel, S.M. Ting, S.B. Samavedam, M. Currie, T.A. Langdo and E.A. Fitzgerald, *J. Vac. Sci. Technol.* **B16**, 1471 (1998).

[12] R.K. Ahrenkiel, M.M. Al-Jassim, B. Keyes, D. Dunlavy, K.M. Jones, S.M. Vernon, and T.M. Dixon, *J. Electrochem. Soc.* **137**, 996 (1990).

[13] J.A. Carlin, S.A. Ringel, E.A. Fitzgerald, M. Bulsara and B.M. Keyes, *Appl. Phys. Lett.* **76**, 1884 (2000).

[14] A. Freundlich, J.C. Grenet, G. Neu, and G. Stobl, *Appl. Phys. Lett.* **59**, 3568 (1991).

[15] N.A. El-Masry, S.A. Hussien, A.A. Fahmy, N.H. Karam, and S.M. Bedair, *Material Letters* **14**, 58 (1992).

[16] M. Yamaguchi and C. Amano, *J. Appl. Phys.* **58**, 3601 (1985).

[17] M. Yamaguchi, A. Yamamoto, ands Y. Itoh, *J. Appl. Phys.* **59**, 1751 (1986).

[18] H. Okamoto, Y. Kadota, Y. Wantanabe, Y. Fukuda, T. Oh'hara, and Y. Ohmachi, *Proc. 20th IEEE Photovolt. Spec. Conf.*, 475 (1988).